METHOD AND APPARATUS FOR POWER OPTIMIZATION DURING INTEGRATED CIRCUIT DESIGN PROCESS

ABSTRACT

Method and apparatus for designing an integrated circuit is described. In an example, the integrated circuit is designed in accordance with timing constraint data. Any logic paths in the plurality of logic paths that have a timing characteristic within a threshold are identified and define a first set of logic paths. Any logic paths in the plurality of logic paths other than those in the first set of logic paths define a second set of logic paths. The integrated circuit is then selectively optimized to reduce power consumption in response to the first set of logic paths and the second set of logic paths. In another example, the integrated circuit is first designed in accordance with timing constraint data. Timing critical logic circuitry is then identified. The integrated circuit is then selectively optimized in response to the timing critical circuitry.